Claims

1. A clock and data recovery unit for recovering a received serial data bit stream having:

(a) phase adjustment means for adjustment of a sampling time in the center of a unit interval (UI) of the received data bit stream, wherein the phase adjustment means comprises:

(a1) means for generating equidistant reference phase signals;

(a2) a phase interpolation unit (PIU) which rotates the generated reference phase signals with a predetermined granularity in response to a rotation control signal;

(a3) an oversampling unit (OSU) for oversampling the received data stream with the rotated reference phase signals according to a predetermined oversampling rate (OSR);

(a4) a serial-to-parallel-conversion unit which converts the oversampled data stream into a deserialized data stream with a predetermined decimation factor (DF);

(a5) a binary phase detection unit (BPD) for detecting an average phase difference (AVG-PH) between the received serial data bit stream and the rotated reference phase signal by adjusting a phase detector gain (PDG) depending on the actual data density (DD) of the deserialized data stream such that the variation of the average phase detection gain (PDG) is minimized; and

(a6) a loop filter for filtering the detected average phase difference (AVG-PH) to generate the rotation control signal for the phase interpolation unit (PIU);

(b) data recognition means (DRM) for recovery of the received data stream which includes a number of parallel data recognition FIR-Filters,wherein each data recognition FIR-Filter comprises:

(b1) a weighting unit for weighting data samples of the deserialized data stream around the sampling time adjusted by the phase adjustment means;

(b2) a summing unit for summing up the weighted data samples; and

(b3) a comparator unit for comparing the summed up data samples with a threshold value to detect the logic value of a data bit within the received serial data bit stream.

2. The clock and data recovery unit according to claim 1 wherein the binary phase detection unit (BPD) comprises:

means for detecting the actual data density of the parallised data bit stream; and

means for adjusting the phase detector gain (PDG) depending on the detected actual data density.

3. The clock and data recovery unit according to claim 2 wherein the means for detecting the actual data density comprises a plurality of EXOR gates,

wherein each EXOR gate compares two neighboring data samples generated by the oversampling unit to decide whether a data transition has occurred.

4. The clock and data recovery unit according to claim wherein the means for detecting the actual data density

further comprises summation means for accumulating the number of transitions detected by the EXOR gates.

5. The clock and data recovery unit according to claim 4 wherein the means for adjusting the phase detector gain calculates the phase detector gain (PDG) by multiplying the accumulated number of transitions with a multiplication factor (MF).

6. The clock and data recovery unit according to claim 5 wherein the multiplication factor (MF) is increased when the detected number of transitions is decreased.

7. The clock and data recovery unit according to claim 3 wherein the number (N) of EXOR gates for detection of the actual data density is given by the product of the decimation factor (DF) of the serial-to-parallel-conversion unit and the oversampling rate (OSR) of the oversampling unit ($N = DF \times OSR$).

8. The clock and data recovery unit according to claim 1 wherein the decimation factor (DF) of the serial to parallel conversion unit is eight ($DF = 8$).

9. The clock and data recovery unit according to claim 1 wherein the oversampling rate (OSR) of the oversampling unit is four ($OSR = 4$).

10. The clock and data recovery unit according to claim 1 wherein the data transmission rate (DR) of the serial data bit stream is more than one Gigabit per second ($DR \geq 1$ Gbit/sec).

11. The clock and data recovery unit according to claim 1 wherein the weighting unit of the data recognition means comprises signal amplifiers, wherein each signal amplifier amplifies a respective data sample with a programmable gain.

12. The clock and data recovery unit according to claim 1 wherein the data recognition FIR-Filters of the data recognition means are connected to a FIFO-memory.

13. The clock and data recovery unit according to claim 1 wherein the number of data recognition FIR-Filters corresponds to the decimation factor (DF) of the serial-to-parallel-conversion unit.

14. The clock and data recovery unit according to claim 1 wherein the oversampling unit (OSU) comprises a predetermined number of clock triggered sampling elements.

15. The clock and data recovery unit according to claim 14 wherein the sampling elements are D-Flip-Flops.

16. The clock and data recovery unit according to claim 14 wherein the sampling elements are D-Latches.

17. The clock and data recovery unit according to claim 14 wherein each sampling element is clocked by a corresponding rotated reference phase signal generated by the phase interpolation unit (PIU).

18. The clock and data recovery unit according to claim 17, wherein the phase interpolation unit (PIU) comprises a phase interpolator and a multiplexer for rotating the phase signals in response to the rotation control signal.

19. The clock and data recovery unit according to claim 1 wherein the delay locked loop (DLL) receives a reference clock signal from a reference clock generator.

20. The clock and data recovery unit according to claim 19 wherein the reference clock generator is a phase locked loop (PLL).

21. The clock and data recovery unit according to claim 1 wherein the loop filter has a PID-characteristic.

22. The clock and data recovery unit according to claim 1 wherein the loop filter is programmable.

23. The clock and data recovery unit according to claim 1 wherein a lock detection unit is provided which detects whether the clock and data recovery unit is locked to the received serial data bit stream.

24. The clock and data recovery unit according to claim 1 wherein a transition loss the detection unit is provided which detects when the serial data bit stream has stopped.

25. The clock and data recovery unit according to claim 1 wherein the phase adjustment means and the data recognition means are integrated in a digital control unit.

26. The clock and data recovery unit according to claim 25 wherein the digital control unit further includes the lock detection unit and the transition loss detection unit.

27. The clock and data recovery unit according to claim 24 wherein a multiplexer for rotating the reference phase signal in response to the rotation control signal is integrated in said digital control unit.

28. The clock and data recovery unit according to claim 1 wherein the equidistant reference phase signals generated by the delay locked loop have a phase difference $\Delta\varphi$ of 45° to define eight phase segments.

29. The clock and data recovery unit according to claim 28 wherein the phase interpolator interpolates phase signals in

each phase segment on the basis of the equidistant reference phase signals.

30. The clock and data recovery unit according to claim 1 wherein the means for generating equidistant reference phase signals are formed by a delay locked loop (DLL).

31. Method for clock and data recovery of a received serial data bit stream comprising the following steps:

(a) adjusting a sampling time in the center of a unit interval (UI) of a received data bit comprising the following substeps:

(a1) rotating generated reference phase signals in response to a rotation control signal;

(a2) oversampling the received data bit stream with the rotated reference phase signals;

(a3) converting the oversampled data bit stream into a deserialized data stream;

(a4) detecting an average phase difference between the received serial data bit stream and the rotated phase signals by adjusting a phase detector gain (PDG) depending on the data density (DD) of the deserialized data stream to minimize the variation of the average phase detector gain;

(a5) filtering the detected phase difference to generate the rotation control signal.

(b) recovering the received data bit stream comprising the following substeps:

(b1) weighting data samples of the parallised data stream around the adjusted sampling time;

(b2) summing up the weighted data samples;

(b3) comparing the summed up weighted data samples with a threshold value to detect the logic value of a data bit within the serial data bit stream.